UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,256	10/30/2003	Chih-Chen Cho	500982.02 (30016/US/2)	9603

27076 7590 04/21/2006

DORSEY & WHITNEY LLP
INTELLECTUAL PROPERTY DEPARTMENT
SUITE 3400
1420 FIFTH AVENUE
SEATTLE, WA 98101

EXAMINER	
THOMAS, TONIAE M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 04/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/699,256	CHO ET AL.	
	Examiner	Art Unit	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18,32,34-37 and 44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-18,32 and 34-37* is/are allowed.

6)☒ Claim(s) *44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *04172006*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action is responsive to the amendment filed on 27 February 2006.

2. Currently, claims 1-18, 32, 34-37, and 44 are pending.

3. The indicated allowability of claim 44 is withdrawn in view of the reference to Cho et al. (US 6,730,553 B2). A rejection based on the Cho et al. reference follows.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claim 44 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 2 of U.S. Patent No.

6,730,553. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 44 recites the following limitations as recited in the patented claim: forming from a nonconductive stack a number of openings to expose a number of semiconductor structures in the array area and in the periphery area, the nonconductive stack including a stopping layer to stop an etching process once etched away to define the bottom of each opening; exposing a portion of a polycrystalline silicon layer in the array area; and filling the number of openings with a conductive stack having the characteristic to reduce a vertical resistance of each semiconductor structure and a horizontal resistance of each semiconductor structure so as to increase the performance of each semiconductor structure.

Reasons for Allowance

6. The following is an examiner's statement of reasons for allowance: the prior art of record does not anticipate, teach or suggest a method for making a semiconductor structure in a substrate having an array area and periphery[1] substantially as claimed, wherein the method comprises at least the steps of: depositing a nonconductive stack over a transistor in the array area and a transistor in the periphery area, the nonconductive stack comprising a stopping layer and a nonconductive layer, respectively; and etching openings by etching the nonconductive stack in at least the array area to expose a

[1] The term "periphery" as used herein is interpreted to mean the peripheral circuitry region of a memory device (see specification page 5, lines 24-27). Likewise, the term "array" as used

polycrystalline silicon layer of the transistor in the array area, as recited in claim 1. Secondly, the prior art of record does not anticipate, teach or suggest a method for making a semiconductor structure in a semiconductor substrate having an array area and periphery substantially as claimed, wherein the method comprises at least the steps of: depositing a nonconductive stack over a gate and source/drain of a memory cell in the array area and over a gate of a transistor in the periphery area, the nonconductive stack comprising a stopping layer and a nonconductive layer, respectively; and removing portions in at least the array that are marked by photolithography to expose a polycrystalline silicon layer of the gate of the memory cell in the array area, as recited in claim 6. Thirdly, the prior art of record does not anticipate, teach or suggest a method for making a semiconductor structure in a substrate having an array area and periphery substantially as claimed, wherein the method comprises at least the steps of: depositing a nonconductive stack having a stopping layer over gates in the array and in the periphery area; and dry etching portions of the array and the periphery until stopped by the stopping layer to expose a portion of the polycrystalline silicon layer of at least one of the gates in the array area and the periphery, as recited in claim 11. Lastly, the prior art of record does not anticipate, teach or suggest a method for forming a routing in a periphery area of a semiconductor structure substantially as claimed, the method comprising forming from a nonconductive stack a trench

---

herein is interpreted to mean the memory cell array of a memory device (see specification page

that superjacently abuts a second gate stack including a polycrystalline silicon layer in the periphery, wherein the nonconductive stack includes a stopping layer that stops an etch process once etched away to define the bottom of the trench and expose at least a portion of the polycrystalline silicon layer of the second gate stack, as recited in claim 32.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday through Friday from 8:30 a.m. to 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TMT
17 April 2006

Mary Wilczewski
Primary Examiner

5, lines 14-16)